CLAIM AMENDMENTS

A listing of an entire set of claims 1-10 is submitted herewith per 37 C.F.R. §1.121. This listing of claims 1-10 will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An integrated circuit comprising:

a plurality of processing elements for executing in parallel at least a subset of a plurality of instructions;

issuing means for configuring the plurality of processing elements by issuing a program-counter-driven instruction flow to the plurality of processing elements; and

configurable interconnection means for connecting each processing element from the plurality of processing elements to at least a subset of other processing elements from the plurality of processing elements;

characterized in that:

the processing elements from the plurality of processing elements are similar to each other, each processing element from the plurality of processing elements being capable of executing each instruction from the plurality of instructions as issued by the issuing means; and

the plurality of processing elements are layed out in a regular grid [[with the issuing means being external to the regular grid]] wherein a distance between a processing element and a neighboring processing element from the plurality of processing elements in a first direction is [[substantially]] the same as a distance between the processing element and a neighboring processing element from the plurality of processing elements in a second direction that is different from the first direction.

2. (Original) An integrated circuit as claimed in claim 1, wherein the integrated circuit comprises a very long instruction word processor architecture and the subset of the plurality of instructions comprises a very long instruction word.

3. (Original) An integrated circuit as claimed in claim 1, characterized in that the configurable interconnection means connect each processing element to each nearest neighboring processing element in the grid.

4. (Original) An integrated circuit as claimed in claim 1 or 3, characterized in that the configurable interconnection means comprise bypassing means for bypassing a processing element from the plurality of processing elements.

5. (Original) An integrated circuit as claimed in claim 1 or 3, characterized in that a processing element from the plurality of processing elements comprises a data storage unit, a function unit and an internal intercommunication network coupling the function unit to the data storage unit.

6. (Original) An integrated circuit as claimed in claim 5, characterized in that the processing element comprises at least a further unit; the function unit, the further unit and the data storage unit being organized as a very long instruction word processor data path.

7. (Original) An integrated circuit as claimed in claim 6, characterized in that the issuing means are distributed over the processing elements.

8. (Previously Amended) A data processing device having an input for receiving a digital data stream and having an output for transmitting a humanly perceptible data result resulting from the digital data stream, characterized in that the input is coupled to the output via an integrated circuit as claimed in any of the claims 1-7, the integrated circuit being arranged for extracting the data result from the digital data stream.

9. (Currently Amended) A method for designing an integrated circuit, the integrated circuit comprising:

a plurality of processing elements for executing in parallel at least a subset of a plurality of instructions;

issuing means for configuring the plurality of processing elements by issuing a program-counter-driven instruction flow to the plurality of processing elements; and

configurable interconnection means for connecting each processing element from the plurality of processing elements to at least a subset of other processing elements from the plurality of processing elements;

characterized by the method comprising the steps of:

designing the processing elements from the plurality of processing elements to be similar to each other, and each processing element from the plurality of processing elements to be capable of executing each instruction from the plurality of instructions as issued by the issuing means;

laying out the plurality of processing elements in a regular grid [[with the issuing means being external to the regular grid]] wherein a distance between a processing element and a neighboring processing element from the plurality of processing elements in a first direction is the same as a distance between the processing element and a neighboring processing element from the plurality of processing elements in a second direction; and

connecting each processing element from the plurality of processing elements to at least a subset of other processing elements from the plurality of processing elements.

10. (Original) A method as claimed in claim 9, characterized in that the step of connecting each processing element from the plurality of processing elements to at least a subset of other processing elements from the plurality of processing elements includes connecting each processing element to each nearest neighboring processing element in the grid